AMENDMENT TO THE CLAIMS

1. (Currently Amended) An apparatus for controlling operations of a synchronous semiconductor memory device, wherein each operation is achieved by a plurality of internal instructions, comprising:

a reference clock block for receiving an external clock and outputting a plurality of delayed clock signals; and

a control block, in response to the plurality of delayed clock signal, for outputting one of the plurality of internal instructions at a first predetermined timing which is earlier than the timing of starting the operation according to an additive latency.

2. (Currently Amended) The apparatus as recited in claim 1, wherein ~~an~~ the additive latency of the synchronous semiconductor memory device is not 0.

3. (Currently Amended) The apparatus as recited in claim 1, wherein the first predetermined timing is earlier ~~one external clock period~~ than the tRCD timing by one external clock period.

4. (Original) The apparatus as recited in claim 1, wherein the plurality of delayed clock signals includes a clock delay signal, a CAS signal, a chip selecting signal, a write enable signal and a RAS signal.

5. (Original) The apparatus as recited in claim 1, wherein the outputted signal from the control block is for controlling whether an inputted column address signal is decoded or not.

6. (Currently Amended) The apparatus as recited in claim 1, further comprising:

an address controller, in response to one of the plurality of delayed clock signal, for outputting an inputted address signal at a second predetermined timing which is earlier than the timing of starting the operation; and

a decoding block for decoding the outputted address signal from the address controller in response to the outputted signal from the control block.

7. (Original) The apparatus as recited in claim 6, wherein the control block includes:

a instruction decoder for outputting an decoded signal after decoding the plurality of delayed clock signal;

a first transmission gate for outputting the decoded signal as the outputted signal when an additive latency is 0 or 1;

first to fourth latches connected serially for sequentially latching the decoded signal;

a second transmission gate for outputting the output signal of the second latch as the outputted signal when the additive latency is 2; and

a third transmission gate for outputting the output signal of the fourth latch as the outputted signal when the additive latency is 3.

8. (Original) The apparatus as recited in claim 7, wherein the address controller includes:

a first transmission gate for outputting the inputted address signal as the internal column address signal when the additive latency is 0 or 1;

a first to fourth latches connected serially for sequentially latching the column address;

a second transmission gate for outputting the output signal of the second latch as the internal column address when the additive latency is 2; and

a third transmission gate for outputting the output signal of the fourth latch as the internal column address when the additive latency is 3.

9. (Currently Amended) A synchronous semiconductor memory device, comprising:

an instruction and address receiving block for receiving an external clock, an external instruction, a row address and a column address and outputting a plurality of internal instructions after decoding the external instruction;

a row address control block, controlled by at least one of the plurality of internal instructions, for decoding the row address;

a column address control block, controlled by at least one of the plurality of internal instructions, for decoding the column address;

a bank for inputting or outputting a data in response to the decoded row and column addresses; and

an I/O block for delivering the data between the bank and an external circuit,

wherein the column address control block includes

a reference clock block for receiving an external clock and outputting a plurality of delayed clock signals; and

a control block, in response to the plurality of delayed clock signal, for performing one among the plurality of internal instructions at a first predetermined timing which is earlier than the timing of starting the operation according to an additive latency.

10. (Currently Amended) The apparatus as recited in claim 9, wherein ~~an~~ the additive latency of the synchronous semiconductor memory device is not 0.

11. (Currently Amended) The apparatus as recited in claim 9, wherein the first predetermined timing is earlier ~~one external clock period~~ than the tRCD timing by one external clock period.

12. (Original) The apparatus as recited in claim 9, wherein the plurality of delayed clock signals includes a clock delay signal, a CAS signal, a chip selecting signal, a write enable signal and a RAS signal.

13. (Original) The apparatus as recited in claim 9, wherein the outputted signal from the control block is for controlling whether an inputted column address signal is decoded or not.

14. (Currently Amended). The apparatus as recited in claim 9, further comprising:

an address controller, in response to one of the plurality of delayed clock signal, for outputting an inputted address signal at a second predetermined timing which is earlier than the timing of starting the operation; and

a decoding block for decoding the outputted address signal from the address controller in response to the outputted signal from~~t~~ the control block.

15. (Original) The apparatus as recited in claim 14, wherein the control block includes:

a instruction decoder for outputting an decoded signal after decoding the plurality of delayed clock signal;

a first transmission gate for outputting the decoded signal as the outputted signal when an additive latency is 0 or 1;

first to fourth latches connected serially for sequentially latching the column address;

a second transmission gate for outputting the output signal of the second latch as the outputted signal when the additive latency is 2; and

a third transmission gate for outputting the output signal of the fourth latch as the outputted signal when the additive latency is 3.

16. (Original) The apparatus as recited in claim 15, wherein the address controller includes:

a first transmission gate for outputting the inputted address signal as the internal column address signal when the additive latency is 0 or 1;

first to fourth latches connected serially for sequentially latching the column address;

a second transmission gate for outputting the output signal of the second latch as the internal column address when the additive latency is 2; and

a third transmission gate for outputting the output signal of the fourth latch as the internal column address when the additive latency is 3.

17. (Currently Amended) A method for controlling operations of a synchronous semiconductor memory device, wherein each operation is achieved by a plurality of internal instructions performing an instruction in response to an additive latency, comprising the step of:

A) receiving an external clock and outputting a plurality of delayed clock signals; and

B) outputting one of the plurality of internal instructions at a first predetermined timing which is earlier than the timing of starting the operation, in response to the plurality of delayed clock signal according to the additive latency.

18. (Currently Amended) The apparatus as recited in claim 17, wherein ~~an~~ the additive latency of the synchronous semiconductor memory device is not 0.

19. (Currently Amended) The apparatus as recited in claim 17, wherein the first predetermined timing is earlier ~~one external clock period~~ than the tRCD timing by one external clock period.

20. (Original) The apparatus as recited in claim 17, wherein the plurality of delayed clock signals includes a clock delay signal, a CAS signal, a chip selecting signal, a write enable signal and a RAS signal.